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Benchmarking quantum error-correcting codes on quasi-linear and central-spin processors

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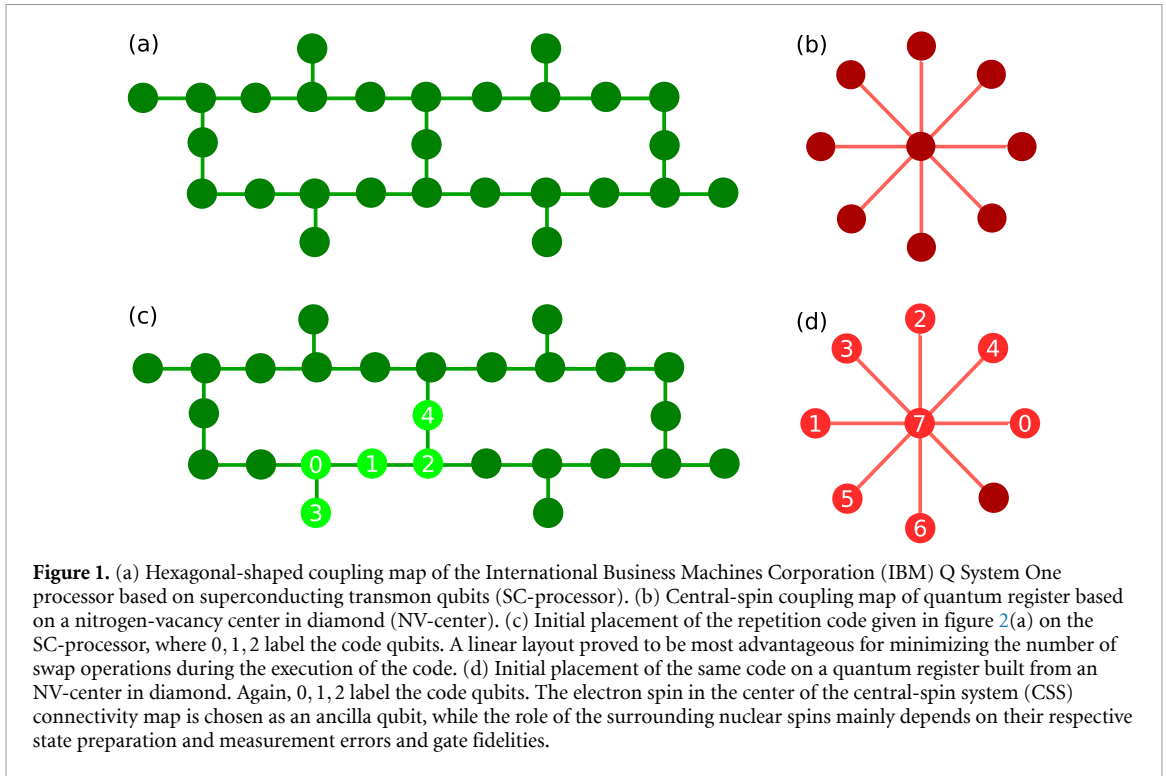**E-mail:** regina.finsterhoelzl@uni-konstanz.de

Abstract

We evaluate the performance of small error-correcting codes, which we tailor to hardware platforms of very different connectivity and coherence: on a superconducting processor based on transmon qubits and a spintronic quantum register consisting of a nitrogen-vacancy center in diamond. Taking the hardware-specific errors and connectivity into account, we investigate the dependence of the resulting logical error rate on the platform features such as the native gates, native connectivity, gate times, and coherence times. Using a standard error model parameterized for the given hardware, we simulate the performance and benchmark these predictions with experimental results when running the code on the superconducting quantum device. The results indicate that for small codes, the quasi-linear layout of the superconducting device is advantageous. Yet, for codes involving multi-qubit controlled operations, the central-spin connectivity of the color centers enables lower error rates.

1. Introduction

The observation and control of coherent quantum systems has advanced rapidly in recent years, leading to a quickened development of quantum technologies in the fields of quantum computing [1–3], quantum simulation [4, 5], and quantum communication [6, 7]. Achievements in the area of quantum computing promise the possibility to ultimately perform computational tasks beyond the reach of high-performance computers [8]. To this end, physical platforms of very different properties are employed, ranging from photonic and atomic [9–12] to solid-state [13–17] systems. However, these noisy intermediate-scale quantum (NISQ) devices are error-prone, making calculations on them imperfect due to gate infidelities and qubit decoherence [18, 19]. For a fully functional, fault-tolerant quantum computer, quantum error-correction (QEC) plays an essential part. It preserves coherence by spreading quantum information on physical qubits using entanglement [2, 3, 20–24]. While the fault-tolerance threshold theorem [25] proves that nearly noise-free computation using noisy components is possible with a moderate qubit overhead, the increase in code size nevertheless makes it difficult to implement QEC codes on NISQ hardware. This led to research efforts to reduce qubit overhead, for instance with the use of flag qubits [26–28] which allow the fault-tolerant constructions of parity checks using a flag qubit indicating errors during the stabilizer measurement, with low-density parity-check codes [29], or by minimizing the qubit overhead in the surface code [30–32]. Recent research predicts requirements for fault-tolerant operations of such small codes or demonstrates their experimental implementation on various hardware platforms [33–42].

Theoretical predictions for the threshold of the physical error rate needed for fault-tolerant operations depend on the used code and error model and vary by several orders of magnitude [43–45]. However, in general, high-precision processor components with error rates $\lesssim 1\%$ are required [24, 30, 46, 47]. Measuring their performance in a reproducible way is thus indispensable and is referred to as benchmarking [48, 49]. Current state-of-the-art techniques include, e.g., randomized benchmarking [50], gate set tomography [51] or quantum state tomography [52], direct fidelity estimation [53] or cross-platform verification [54]. These

Figure 1. (a) Hexagonal-shaped coupling map of the International Business Machines Corporation (IBM) Q System One processor based on superconducting transmon qubits (SC-processor). (b) Central-spin coupling map of quantum register based on a nitrogen-vacancy center in diamond (NV-center). (c) Initial placement of the repetition code given in figure 2(a) on the SC-processor, where 0, 1, 2 label the code qubits. A linear layout proved to be most advantageous for minimizing the number of swap operations during the execution of the code. (d) Initial placement of the same code on a quantum register built from an NV-center in diamond. Again, 0, 1, 2 label the code qubits. The electron spin in the center of the central-spin system (CSS) connectivity map is chosen as an ancilla qubit, while the role of the surrounding nuclear spins mainly depends on their respective state preparation and measurement errors and gate fidelities.

methods differ in complexity, assumption strength, and information gain, and the obtained benefit depends on the problem at hand.

The work presented in this paper investigates the performance of small error-correcting codes transpiled on two solid-state hardware platforms with very different native connectivity, gate sets, and coherence times: a processor built with superconducting transmon qubits featuring a quasi-linear connectivity and a hybrid spintronic quantum register based on defects in diamond with a central-spin system (CSS) connectivity (figure 1). Thus, we compare the central-spin topology and characteristic properties of the nitrogen-vacancy (NV)-center—which is a currently intensely studied hardware resource in the quantum technologies context—with the properties of a technologically further advanced solid-state platform, a superconducting processor, where we relate to the technology using a heavy hexagonal layout. The target quantity for the comparison is the logical error rate—the probability for the error-correcting process to fail, thus the infidelity between the ideal $|\psi\rangle_{\text{ideal}}$ and the noise output state ρ_{out} of the calculation—which we also use to benchmark our predictions with experimental results. The reason for choosing this quantity is the central role it plays in quantum error correction: Here, the aim is to achieve logical error rates below the noise level of the individual components p_e. This reduction of the logical error rate also plays a central role for fault-tolerant computation, where a code correcting a single error is required to yield a logical error rate $\bar{p} = Cp_e^2 < p_e$ (where C is a constant depending on the number of potentially faulty locations in the code), such that with r concatenation steps, the rate may be pushed to $\sim p^{2^r}$ with a moderate overhead—thus, nearly error-free quantum computation may be achieved [23]. We show that the superconducting processor achieves better error rates for small codes while for codes involving multi-qubit controlled operators with weight $w > 2$, a fundamental operation not only in quantum error correction but also for instance in quantum simulation or fault-tolerant quantum computing [2, 55, 56], the native gates and connectivity of the spintronic register prove advantageous.

Superconducting qubits belong to the technologically more advanced platforms [16, 57–60]. They consist of collective excitations in superconducting circuits, where the transmon qubit is built by a parallel circuit consisting of a nonlinear Josephson junction and a capacitor forming a non-equidistant energy spacing. The qubit levels are the lowest ones, resonant at 5 GHz, where microwave pulses realize single-qubit operations [61]. Transmon qubits feature a direct or mediated capacitive nearest-neighbor coupling [16], for instance realized by the cross-resonance gate, which is equivalent to a controlled-NOT (CNOT) gate up to single qubit rotations [57, 62–64]. This allows the construction of planar one- and two-dimensional arrays (figure 1(a)). Readout may be performed using a linear superconducting resonator coupled to the transmon circuit.

The properties of defect-based quantum registers in solids differ in several aspects. Here, we consider the case of a register based on the NV-center in diamond, where one carbon atom has been replaced by a nitrogen

atom (^{14}N) while one of its nearest-neighbor sites is vacant [33, 65–68]. Qubits are based on the NV electron spin as well as on the nuclear spins of the intrinsic ^{14}N atom and the surrounding dilute ^{13}C carbon atoms to which the electron spin couples via the hyperfine interaction. A magnetic field lifts the degeneracy such that the qubit levels may be defined as $m_{s/N} \in [0, -1]$ with transition energies in the range of GHz (MHz) for the electron (nuclear) spins. Microwave (radio frequency) pulses are used for single- or multi-qubit conditional rotations [69–71]. The individual sensing of up to 27 nuclear spins via the electron spin, the full control of up to 9 nuclear spins as well as ultra-long coherence times have been demonstrated experimentally [33, 69, 72–74]. The system is initialized [75, 76] and read out [33, 77–79] optically via the electron spin and its coupling to the nuclear spins [33, 72, 80], enabling the native connectivity of a CSS where the electron spin mediates all couplings (figure 1(b)). Table 1 compares fidelities and coherence times of both platforms.

The experimental implementation of quantum error-correcting codes has been successfully demonstrated on both solid-state systems. While noise-resilient universal sets of single-qubit and multi-qubit gate operations [82, 83] as well as its efficient use for quantum simulations [84] have been predicted for the NV-center, the minimal five-qubit code [85, 86] has been implemented on a seven-qubit register [33] making use of a recently proposed scheme using flag qubits [26–28]. Prior to that, the three-qubit repetition code has been realized as a bit-flip or phase-flip correcting code [69, 70, 80], and encoding into a decoherence-protected subspace has been shown [87]. On the superconducting hardware, the three-qubit repetition code has been implemented successfully [88, 89], while currently, the surface code is heavily explored, making use of the native 2d-planar connectivity of the transmon qubits [34, 90–92].

This paper is structured as follows: in section 2.2, we introduce the two physical platforms used for the benchmark and explain the implemented error model. In section 3, we introduce the error-correcting codes and show our results, followed by a conclusion and outlook in section 5.

2. Model and methods

2.1. Quantum processors
The prediction of the logical error rate achieved by the error-correcting codes is based on an error model built on calibration data. To benchmark this error model, we compare the simulation against the performance of the real quantum processor. For this, we make use of the latest processor generation built by IBM Research, the IBM Q Falcon processor [93] which features a hexagonal connectivity [94], see figure 1(a). In order to benchmark the performance of the transpiled codes, we also use the calibrated data of a specific NV-center operated by a group at the University of Stuttgart [74]. Its native coupling map is CSS-like, where the central electron spin mediates all qubit-qubit interactions, see figure 1(b). The calibration data for both devices is listed in table 2. Gate fidelities are obtained using randomized Clifford benchmarking techniques for both platforms [95–97].

Contrary to the SC-processor which is operated at $T_{op} = 15$ mK, the data for the NV-center is obtained at $T_{op} = 300$ K. State-preparation and measurement errors p_{spam} are in the range of a few percent for both platforms. Gate times T_{gate} are up to two orders of magnitude shorter for the SC-processor, while also the single (two)-qubit gate fidelities F_1 (F_2) differ in the same range, thus are more favorable on the SC-processor. Further improvement of the gate performance of the NV-center operations could be achieved e.g. using optimal control theory, as the higher fidelities listed in table 1 indicate, which have been demonstrated at room temperature on the electron and nitrogen spin. Contrary to this, the coherence times are up to several orders of magnitude higher on the NV-center. The spin relaxation times T_1 depend on the charge state and the spin type of the NV-center. In the negatively charged (NV$^-$) state, the NV nuclear spins have relaxation times $T_1 \gtrsim 250$ ms.

Single native gates are the NOT gate (X) and its square root SX on the SC-processor, and rotations around the x-axis (RX) and y-axis (RY) on the NV-center. Native two-qubit gates are the CNOT gate on the superconducting hardware and the controlled-rotations gate along the x- and y-axis on the NV-center. For both platforms, the RZ gate may be executed virtually by shifting the phase of the drive accordingly. As this does not require additional pulses, the gate is considered perfect ($F = 1.0$) with zero gate time.

2.2. Error model
To simulate the impact of decoherence on the circuit performance, we make use of an error model specified for each device building on calibrated data [100–102]. The errors are assumed to be uncorrelated and are described by noisy quantum channels $\mathcal{E}(\rho)$ acting on the density matrix ρ. In the operator-sum representation, they are given by

$$\mathcal{E}(\rho) = \mathrm{Tr}_{env}\left[\mathcal{U}(\rho \otimes \rho_{env})\mathcal{U}^\dagger\right] = \sum_k E_k \rho E_k^\dagger, \tag{1}$$

Table 1. Comparison of important properties of two different hardware candidates for gate-based quantum computing: superconducting transmon qubits (SC) [16, 61, 64] and spintronic qubits [70–72, 78, 81] consisting of an NV-center in diamond. T_2^{Hahn} denotes the spin-echo time measured by Hahn-type experiments, while F_1 (F_2) indicates the single-qubit (two-qubit) gate fidelity and T_{op} the operating temperature of the system. The spintronic hardware features very long coherence times (obtained at 3.7 K). Contrary to the transmon processor which needs cryogenic technology and operating temperatures in the range of mK, the NV-center may be operated at higher temperatures up to 300 K (see table 2 for the corresponding parameters). While high-fidelity gates have been demonstrated both on the NV-center register as well as on transmon qubits, the former have been achieved at room temperature. The coherence time may be extended to over a minute for the nuclear spins [72] and to one second for the electron spin [78] using dynamical decoupling techniques. Note that the NV-center gate fidelities depend on the used spin type (see table 2), while the fidelities listed here have been obtained for the electron and intrinsic nitrogen nuclear spin.

Qubit platform	T_2^{Hahn} (ms)	F_1	F_2	T_{op} (K)
SC	0.1 [16, 64]	0.9992 [61]	0.994 [64]	1.5×10^{-2}
NV-center	Electron spin: 1.18 [70] ^{14}N-spin: 2300 [33, 72] ^{13}C-spin: 260–770 [33, 72]	0.99 995 [71]	0.992 [71]	3.7–300

Table 2. Calibration data for the superconducting quantum processor IBM Q Falcon (SC-processor) [93] and a quantum register based on an NV-center in diamond [74, 98], both employed for benchmarking. T_2^{Hahn} times are spin-echo times obtained with Hahn-type experiments [74, 99]. Contrary to the SC-processor which is operated at $T_{\mathrm{op}} = 15$ mK, the data for the NV-center is obtained at $T_{\mathrm{op}} = 300$ K. State-preparation and measurement errors p_{spam} are in the range of a few percent for both platforms. Gate times T_{gate} are up to two orders of magnitude shorter for the SC-processor, while also the single (two)-qubit gate fidelities F_1 (F_2) differ in the same range and are thus more favorable on the SC-processor. The gate performance of the NV-center operations could be further improved e.g. using optimal control theory, as the fidelities listed in table 1—which have been demonstrated at room temperature—indicate. Contrary to this, the coherence times are up to several orders of magnitude higher for the NV-center. Note that T_1 strongly depends on the charge state and the spin type of the NV-center.

	NV-center		SC-processor
	Electron spin	Nuclear spin	
T_1 (ms)	5.7	$\gtrsim 250$	0.1
T_2^{Hahn} (ms)	0.4	0.9	0.1
T_{gate} (ms)	0.001–0.15		0.0005
$1 - F_1$	0.02		0.0008
$1 - F_2$	0.05		0.01
T_{op} (K)	300		1.5×10^{-2}
p_{spam}	0.02–0.04		0.02–0.04

where the Kraus operators $\{E_k\}$ fulfill $\sum_k E_k^\dagger E_k = \mathbb{I}$. Here, the map $\mathcal{E}(\rho)$ is completely positive and non-trace increasing. Note that the Kraus operators are not uniquely determined by $\mathcal{E}(\rho)$ [2]. In addition to the SPAM errors, decoherence is modeled by taking qubit relaxation as well as errors due to faulty gates into account. Here, relaxation errors are assumed to occur due to amplitude damping and dephasing processes. Amplitude damping describes the effect of energy dissipation into the environment of a qubit [57, 103]. Phase damping describes the loss of information about the relative phases between the energy eigenstates into an environment, but does not affect the population of the eigenstates. When combined into a single quantum operation, the Kraus operators describing both amplitude and phase damping read as [104] (see appendix A)

$$E_{\mathrm{apd},0} = \begin{pmatrix} 1 & 0 \\ 0 & \sqrt{1-p_{\mathrm{ad}}}\sqrt{1-p_{\mathrm{pd}}} \end{pmatrix}, E_{\mathrm{apd},1} = \begin{pmatrix} 0 & \sqrt{p_{\mathrm{ad}}} \\ 0 & 0 \end{pmatrix}, \tag{2}$$

$$E_{\mathrm{apd},2} = \begin{pmatrix} 0 & 0 \\ 0 & \sqrt{1-p_{\mathrm{ad}}}\sqrt{p_{\mathrm{pd}}} \end{pmatrix}. \tag{3}$$

Here, we may relate the probability for the qubit to lose an excitation into the environment p_{ad} and the probability for the qubit to experience a random phase kick p_{pd} to the relaxation time T_1, the decoherence time T_2, and the gate time Δt, with

$$1 - p_{\mathrm{ad}} = e^{-\Delta t/T_1}, \sqrt{1-p_{\mathrm{ad}}}\sqrt{1-p_{\mathrm{pd}}} = e^{-\Delta t/T_2}. \tag{4}$$

Gate errors are captured with the depolarizing channel, where with probability p_{depol}, the density matrix ρ is replaced with a completely mixed state according to $\mathcal{E}_{\mathrm{depol}}(\rho) = p_{\mathrm{depol}}/d\,\mathbb{I} + (1-p_{\mathrm{depol}})\rho$. This results in the four Kraus operators $E_0 = \sqrt{1-3p_{\mathrm{depol}}/4}\,\mathbb{I}$, $E_1 = \sqrt{p_{\mathrm{depol}}}/2\,X$, $E_2 = \sqrt{p_{\mathrm{depol}}}/2\,Y$ and $E_3 = \sqrt{p_{\mathrm{depol}}}/2\,Z$, where

X, Y, Z represent the standard Pauli matrices $\sigma_x, \sigma_y, \sigma_z$, respectively. Lastly, SPAM-errors are modeled with a standard Pauli bit-flip channel which captures the probability of the qubit being prepared or measured in the $|1\rangle$ instead of the $|0\rangle$ state (and vice versa). It is applied before an ideal measurement operation $\mathcal{E}_{\mathrm{m,ideal}}$:

$$\mathcal{E}_{\mathrm{m}} = \mathcal{E}_{\mathrm{m,ideal}} \circ \mathcal{E}_{\mathrm{spam}}, \quad \mathcal{E}_{\mathrm{spam}}(\rho) = p_{\mathrm{spam}} X \rho X + (1 - p_{\mathrm{spam}})\rho. \tag{5}$$

Noisy single-qubit gates consist of an ideal, unitary gate U followed by the quantum noise channels, thus $\mathcal{U} \rightarrow \mathcal{E}_{\mathrm{damp}} \circ \mathcal{E}_{\mathrm{depol}} \circ \mathcal{U}$. Errors on N-qubit gates $\mathcal{U}^{(N)}$ are assumed to occur uncorrelated on the single qubits (indexed with i) upon which U acts non-trivially, thus

$$\mathcal{U}^{(N)} \rightarrow \bigotimes_{i=0}^{N-1} \mathcal{E}_{\mathrm{damp},i} \circ \bigotimes_{i=0}^{N-1} \mathcal{E}_{\mathrm{depol},i} \circ \mathcal{U}^{(N)}. \tag{6}$$

Note that we apply the ideal identity to spectator qubits, thus we do not include their free decay in the model, as their protection against decoherence by dynamical decoupling has been demonstrated experimentally for both platforms [33, 72, 105, 106]. Including them would lead to an increase of the simulated error rate in both cases and would not affect our results qualitatively. Also note that while the model does not capture spatially correlated errors such as crosstalk on the superconducting processor or fluctuations due to the coupling of the nuclear spins to the central electron spin for the NV-center, the model captures the decoherence processes very well and remaining errors are small in almost all cases (see section 3.2).

2.3. Model parameterization
Based upon these assumptions, the model is adaptive to the respective hardware by capturing its native connectivity, coherence times, and gate errors using calibrated data. Thus, the noise models we use for simulating the respective hardware behavior capture the essential differences between both platforms. To this end, we make use of the relationship between the average gate fidelity F and the Kraus operators of a quantum operation [107, 108] given by

$$F(\mathcal{E}, U) = \int d\psi \langle \psi | U^{\dagger} \mathcal{E}(U|\psi\rangle\langle\psi|U^{\dagger}) U | \psi \rangle = \frac{\sum_k |\mathrm{Tr}(E_k)|^2 + d}{d(d+1)}, \tag{7}$$

where U represents the target unitary and $\mathcal{E} = \sum_k E_k \rho E_k^{\dagger}$ a quantum channel with dimension d characterizing the noise. Note that from (7) follows that $F = F(\mathcal{E})$, the average gate fidelity only depends on the noise channel. The average gate infidelity is given as the total gate error p_{g}, which is obtained for each qubit and each native gate from calibrated data. We first calculate the average gate fidelity due to relaxation processes $F(\mathcal{E}_{\mathrm{damp}})$ from (7) using the parameters T_1, T_2 and Δt. Next, we approximate the remaining gate error as $p_{\mathrm{g}} = (1 - F(\mathcal{E}_{\mathrm{damp}})) + (1 - F(\mathcal{E}_{\mathrm{depol}}))$, and subsequently choose p_{depol} such that $1 - F(\mathcal{E}_{\mathrm{depol}}) = F(\mathcal{E}_{\mathrm{damp}}) - (1 - p_{\mathrm{g}})$. Thus we approximate the total gate error as a sum of the infidelities resulting from both error processes. By also taking the native connectivity map into account, we obtain an error model specific to each device for the simulator.

2.4. Qubit routing
The translation of a quantum circuit into a circuit adapted to the respective native gates, memory layout, and error characteristics of a hardware platform is called transpilation or the qubit routing problem [109–112]. Transpiling a quantum circuit in an optimal way is crucial for the reduction of the impact of noise—the task is to maximize the fidelity of the transpiled circuit. However, both finding the optimal initial layout as well as the optimal swapping sequences during the execution of the circuit are NP-hard combinatorial problems and thus come with very high computational costs, at least for larger circuits and devices. Additional resources are needed as both problems are intertwined and depend on the native gate set as well as on the gate fidelities of the given device. In recent years, many numerical solutions have been proposed for instance based on stochastic optimization [113, 114] or machine learning methods [115, 116].

In order to understand the hardware-specific impact of each of the limiting factors such as the native gate set, native topology, and gate errors on the transpilation process, we transpile the circuit in steps, using analytical methods where possible, and check our result using numerical techniques provided by the open-source framework qiskit [100]. First, we transpile the virtual circuit to the native gates and minimize the circuit depth using circuit identities [2] and the reduction of the number of circuit layers [109]. We minimize the counts of the operation with the lowest fidelity, which are multi-qubit gates for both platforms. Where possible, we make use of mid-circuit projective measurements, combined with post-processing [117],

to reduce the impact of noisy gates on the result. Next, we evaluate the optimal placement of the virtual qubits on the physical device. This corresponds to minimizing the number of additionally inserted SWAP gates while routing the qubits on the native topology of the device. As the SWAP operation is not native on either platform, it has to be transpiled at the cost of three CNOT gates with $\text{SWAP}(q_0, q_1) = \text{CNOT}(q_0, q_1)\text{CNOT}(q_1, q_0)\text{CNOT}(q_0, q_1)$ for two qubits labeled q_0 and q_1.

We describe the native device connectivity as a directed graph, and for all subgraphs of different connectivity depending on the symmetry of the processor layout, we evaluate the initial layout requiring the least number of SWAP operations, which corresponds to providing the maximal number of native multi-qubit gates required in the specific circuit. When using post-processing, we choose the layout which enables us to perform as few operations after the projective measurement step as possible. Finally, we use the error model to find the optimal placement of the subgraph on the hardware. Here, we calculate the average error rate p_{av} with $p_{\text{av}} = 1 - \Pi_{i=0}^{N-1} F_i$ with N the number of noisy operations in the transpiled circuit. Figure 1 depicts initial layout on the SC-processor (1(c)) and on the NV-center (1(d)) for an repetition code using three code qubits.

3. Results

3.1. Repetition codes

We employ two fundamental error-correcting codes: the three-qubit repetition code fully correcting single bit-flip errors (bit-flip code) and the rotated three-qubit repetition code fully correcting single phase-flip errors (phase-flip code). Both codes have the advantage of requiring a low number of physical qubits. They are depicted in figures 2(a) and (b). The repetition code encodes the state $|\psi\rangle$ on a single physical qubit into the code space of three qubits with $|\psi\rangle = \alpha|0\rangle + \beta|1\rangle \rightarrow |\psi\rangle_L = \alpha|000\rangle + \beta|111\rangle \equiv \alpha|0\rangle_L + \beta|1\rangle_L$, see figure 2(a). Any bit-flip error occurring on the encoded qubit may be corrected by measuring the stabilizers $Z_1 Z_2$ and $Z_2 Z_3$ which will force the system into one of their eigenstates. If $|\psi\rangle_L$ is in the code space, the result of both stabilizer measurements will yield $+1$ and leave the state undisturbed, while if an error has occurred, the measured syndrome will yield a negative eigenvalue -1 on one or both stabilizers. The result will indicate the required recovery procedure which implies a quantum operation conditioned on the measurement outcome. The phase-flip code may be described as a rotated bit-flip repetition code, where the quantum state is encoded as $\alpha|0\rangle + \beta|1\rangle \rightarrow \alpha|{+}{+}{+}\rangle + \beta|{-}{-}{-}\rangle$. The stabilizers read as $X_1 X_2, X_2 X_3$ accordingly. The code is given in figure 2(b), its steps are equivalent to the ones of the bit-flip code explained above.

As it is generally the case in QEC, both circuits include a feed-forward operation, where the classical measurement result conditions the quantum operation during runtime. As this operation is not yet available on either of the processors employed here [118], we implement the recovery either by post-processing or by unitary correction. In the former case, the syndrome indicates a classical correction of the result of the quantum computation (figure 3(a)), while the latter implements the correction using multi-qubit conditioned quantum gates (figure 3(b)).

3.2. Benchmarking the model

We use the bit-flip code including post-processing for benchmarking the error model. To this end, we deliberately induce a random bit-flip error on one of the code qubits during the noise evolution and evaluate its correct detection using the syndrome. We transpile the circuit to both hardware platforms (see section 2.4) using the calibrated data described in section 2.1. On the given topology of the superconducting device, all connected subgraphs are of linear or nearly linear connectivity. Interestingly, the number of CNOT gates in the code is minimal when transpiled to the linear connectivity, as this layout provides all native two-qubit gates which are required after the intermediate measurement step. Also, it enables multi-qubit gate cancellation, as two sequential identical CNOTs form the identity according to $\text{CNOT}(q_0, q_1)\text{CNOT}(q_0, q_1) = \mathbb{I}$. Figure 1(c) depicts a possible initial placement of the virtual qubits on the physical device. The resulting circuit transpiled for the superconducting device is depicted in figure 4.

We benchmark the noise model with the behavior of the real quantum device. The results are depicted in figure 5. The model qualitatively captures the behavior of the quantum device well and the remaining deviations between model and experiment are small. Here, the error rate predicted by the simulator generally lies slightly below the one obtained by the experiment, while for some cases, the prediction is too low. The main reason for these deviations is presumably that the model is built from uncorrelated error types which are hardware agnostic and thus fail to capture hardware-specific, spatially correlated processes such as cross-talk [119]. It could be adapted to the specific hardware for instance using neural networks trained to the specific errors as demonstrated in [101]. However, in order to use the error model for benchmarking, we
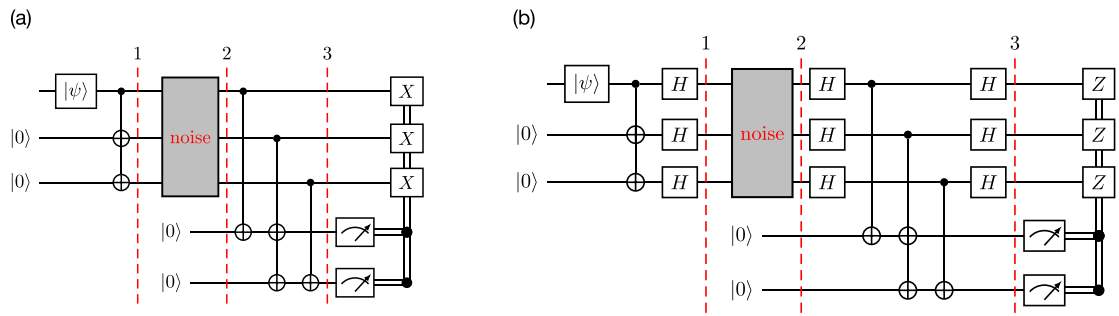
Figure 2. (a) Circuit representation of the three-qubit repetition code correcting a single bit-flip error. It encodes the state $|\psi\rangle$ on a single physical qubit into the code space of three qubits with $|\psi\rangle = \alpha|0\rangle + \beta|1\rangle \rightarrow |\psi\rangle_L = \alpha|000\rangle + \beta|111\rangle \equiv \alpha|0\rangle_L + \beta|1\rangle_L$ (first part until line 1). Any bit-flip error occurring on the encoded qubit (line 1–line 2) may be corrected by measuring the stabilizers $Z_1 Z_2$ and $Z_2 Z_3$ which will force the system into one of their eigenstates (until line 3). If $|\psi\rangle_L$ is in the code space, the measurement in the last section of the circuit will yield the eigenvalues $+1$ and leave the state undisturbed, while if an error has occurred, the measured syndrome will indicate the required recovery procedure. (b) The rotated three-qubit repetition code correcting single phase errors. Its structure is equivalent to the bit-flip code. First, the state $|\psi\rangle$ is encoded in the logical state space with $|\psi\rangle = \alpha|0\rangle + \beta|1\rangle \rightarrow |\psi\rangle_L = \alpha|++\,+\rangle + \beta|--\,-\rangle \equiv \alpha|0\rangle_L + \beta|1\rangle_L$, and is then exposed to noisy evolution. With the following parity check using the stabilizers $X_1 X_2$ and $X_2 X_3$, phase-flip errors may be detected and corrected with Z-gates conditioned on the measurement result.
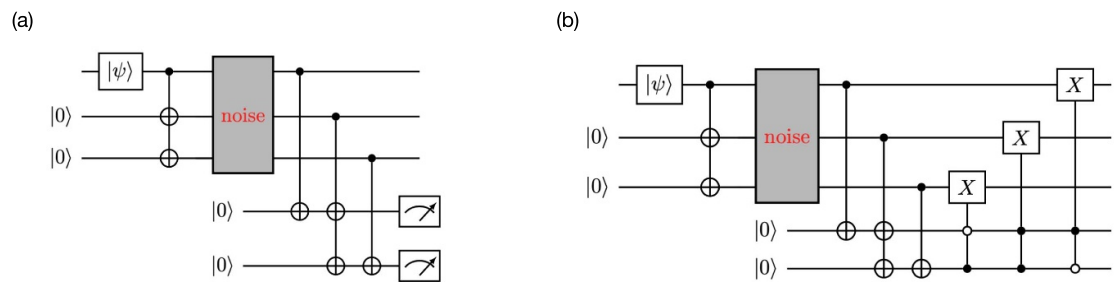

Figure 3. Error-recovery procedure without feed-forward on the example of the bit-flip code. (a) Classical post-processing, where the syndrome indicates a classical correction of the result of the quantum computation. (b) Circuit using unitary correction by multi-qubit conditioned quantum gates.
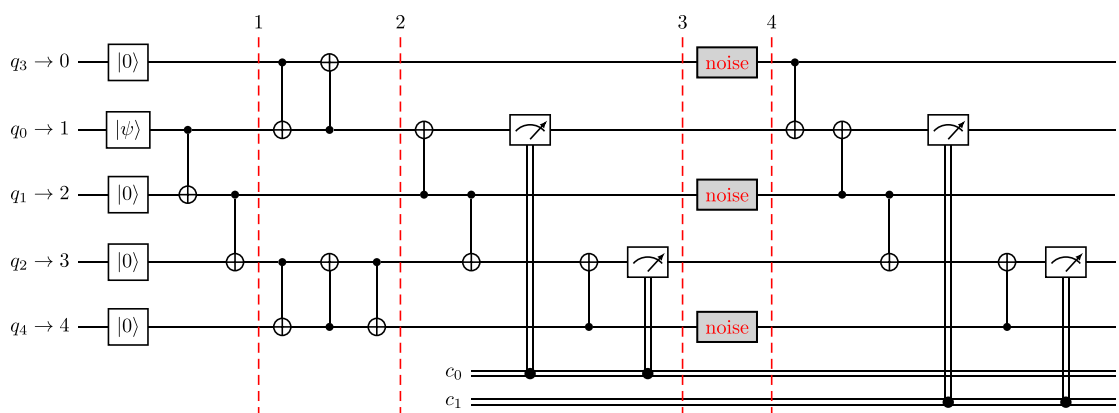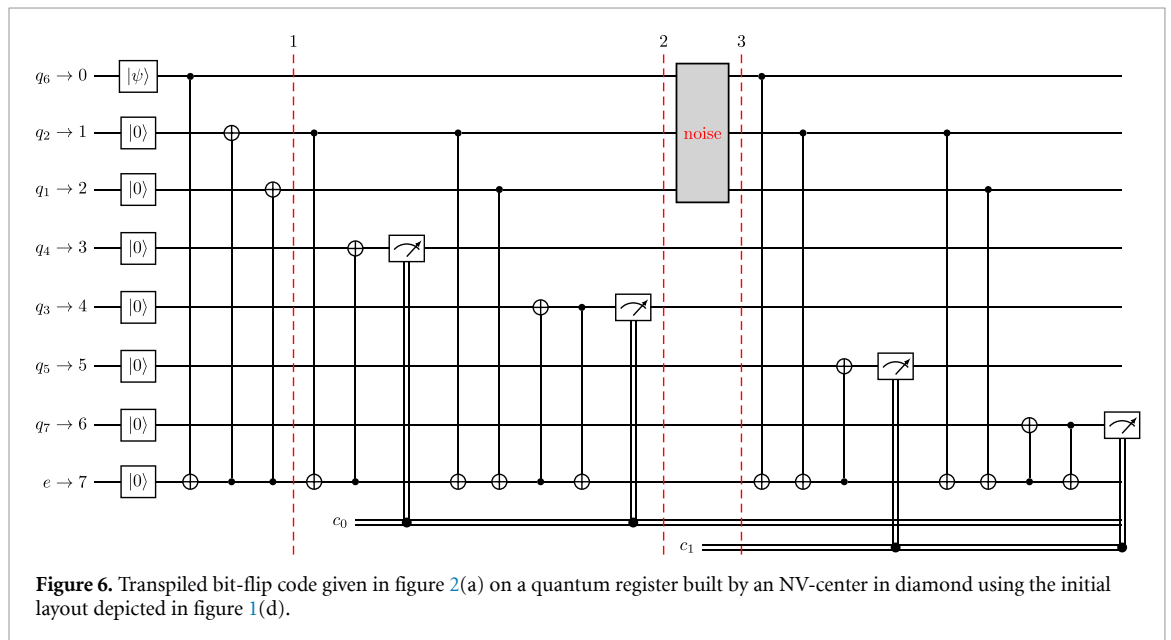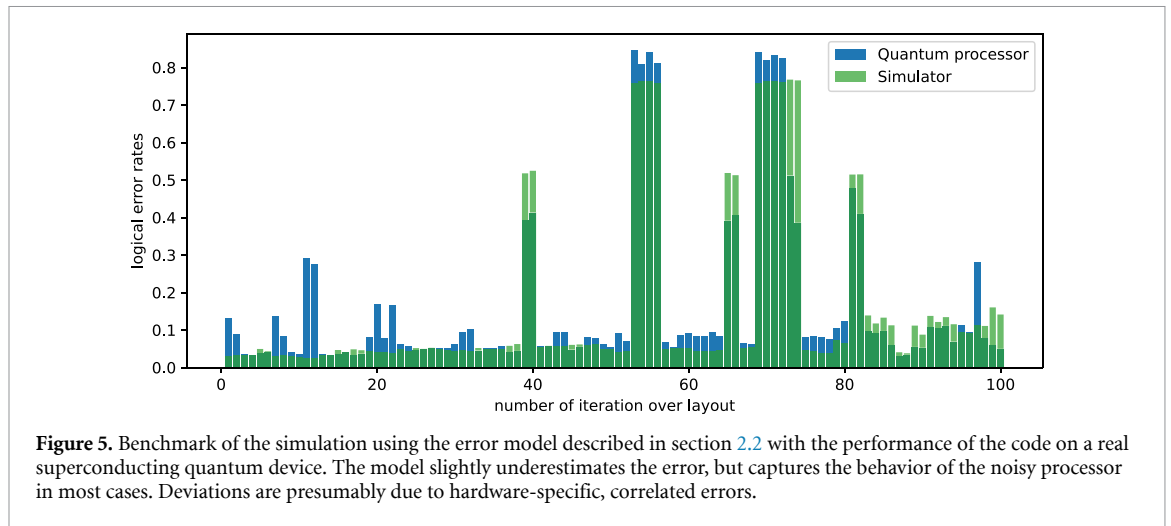

Figure 4. Transpiled bit-flip code given in figure 2(a) on the superconducting processor using the initial layout depicted in figure 1(c). The number of CNOT gates in the code is minimal when transpiled to the linear connectivity, as this layout provides all native two-qubit gates which are required after the intermediate measurement step.

Figure 5. Benchmark of the simulation using the error model described in section 2.2 with the performance of the code on a real superconducting quantum device. The model slightly underestimates the error, but captures the behavior of the noisy processor in most cases. Deviations are presumably due to hardware-specific, correlated errors.

Figure 6. Transpiled bit-flip code given in figure 2(a) on a quantum register built by an NV-center in diamond using the initial layout depicted in figure 1(d).

require the error channels to be adaptable to the specific properties of the respective platform, as described above due to a lack of data we can benchmark the model only on the superconducting platform, thus we require the model to be build from more general quantum channels which allow the adaptation to the hardware using calibrated data.

3.3. Performance of the bit-flip code

Next, we use the benchmarked error model to evaluate the performance of the bit-flip code comparatively on both platforms. To this end, we transpile the code also to the NV-center native properties. Figure 6 depicts the transpiled circuit, while figure 1(d) depicts the initial layout. The central electron spin is chosen as ancilla qubit. Again, the first part until line 1 depicts the encoding, the projection into code space (line 1–line 2) followed by the random bit-flip error (line 2–line 3). The part until line 4 depicts the stabilizer measurement. Due to the native connectivity, the central spin serves as a mediator both for the entangling gates and readout. Note that the CSS-like connectivity map is less favorable in this case when compared to the quasi-linear layout of the SC-processor. While in the latter case, the transpiled circuit only requires three CNOTs for measuring the stabilizers, their number rises to seven CNOTs in the case of the NV-center register. Again, we run the code on the simulator. The best results of both systems are depicted in figure 7. Clearly, the code performs better on the superconducting hardware. Here, the best results reach a logical
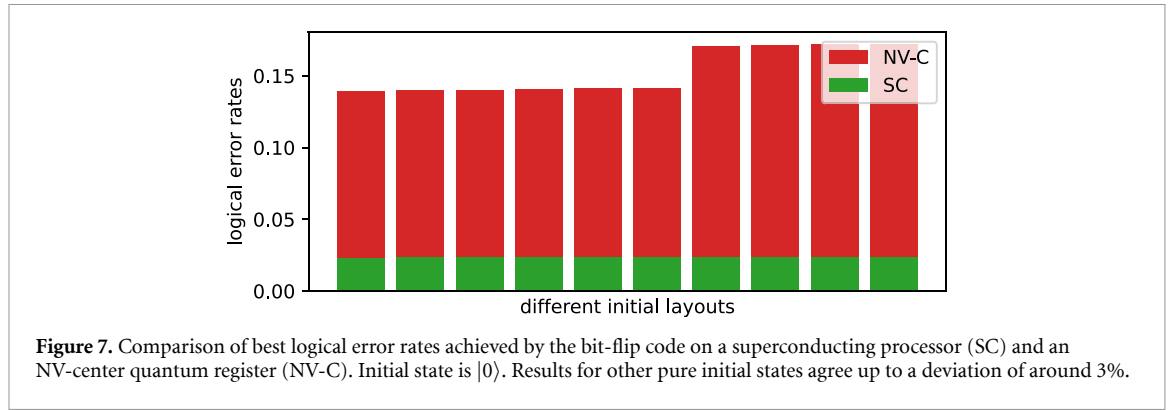
Figure 7. Comparison of best logical error rates achieved by the bit-flip code on a superconducting processor (SC) and an NV-center quantum register (NV-C). Initial state is $|0\rangle$. Results for other pure initial states agree up to a deviation of around 3%.
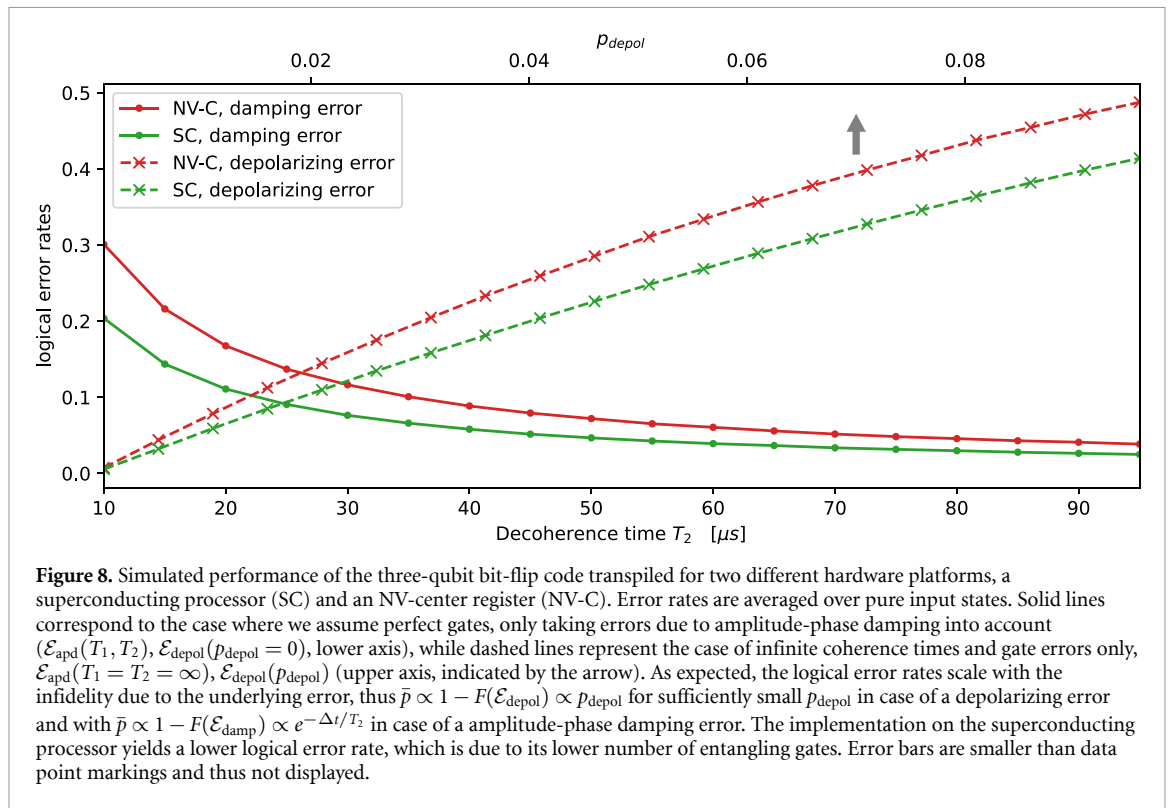

Figure 8. Simulated performance of the three-qubit bit-flip code transpiled for two different hardware platforms, a superconducting processor (SC) and an NV-center register (NV-C). Error rates are averaged over pure input states. Solid lines correspond to the case where we assume perfect gates, only taking errors due to amplitude-phase damping into account $(\mathcal{E}_{\mathrm{apd}}(T_1, T_2)), \mathcal{E}_{\mathrm{depol}}(p_{\mathrm{depol}} = 0)$, lower axis), while dashed lines represent the case of infinite coherence times and gate errors only, $\mathcal{E}_{\mathrm{apd}}(T_1 = T_2 = \infty), \mathcal{E}_{\mathrm{depol}}(p_{\mathrm{depol}})$ (upper axis, indicated by the arrow). As expected, the logical error rates scale with the infidelity due to the underlying error, thus $\bar{p} \propto 1 - F(\mathcal{E}_{\mathrm{depol}}) \propto p_{\mathrm{depol}}$ for sufficiently small p_{depol} in case of a depolarizing error and with $\bar{p} \propto 1 - F(\mathcal{E}_{\mathrm{damp}}) \propto e^{-\Delta t/T_2}$ in case of a amplitude-phase damping error. The implementation on the superconducting processor yields a lower logical error rate, which is due to its lower number of entangling gates. Error bars are smaller than data point markings and thus not displayed.

error rate of 0.023 compared to 0.139 on the NV-center. In order to compare the influence of certain types of errors—those due to limited coherence times and those due to gate imperfections—we evaluate the impact of both errors separately. To this end, we build the model with equal parameters for both systems, enabling a comparison of the influence of the native gates and native connectivity. First, we assume perfect gates and only take errors due to amplitude-phase damping into account, and average over all input states, see figure 8 (solid lines). The superconducting processor outperforms the NV-center. This is also the case if only depolarizing gate errors are considered (dashed lines). Note that as expected, the logical error rates scale with the infidelity due to the underlying error, thus $\bar{p} \propto 1 - F(\mathcal{E}_{\mathrm{depol}}) \propto p_{\mathrm{depol}}$ for sufficiently small p_{depol} in case of a depolarizing error and with $\bar{p} \propto 1 - F(\mathcal{E}_{\mathrm{damp}}) \propto e^{-\Delta t/T_2}$ in case of a amplitude-phase damping error.

3.4. Results for the phase-flip code
Next, we investigate the performance of the phase-flip code. Here, we correct the error unitarily, as depicted in figure 3(b). In the same manner as described in section 3.3, we use an equal parameter set on both systems, and take the native gates and the native connectivity into account. This allows us to additionally extend the list of basis gates of the NV-center to the uncalibrated $C^{(2)}$ and $C^{(3)}$ gates which are native on the NV-center register. Their usage has been demonstrated in quantum error-correcting experiments [69]. We
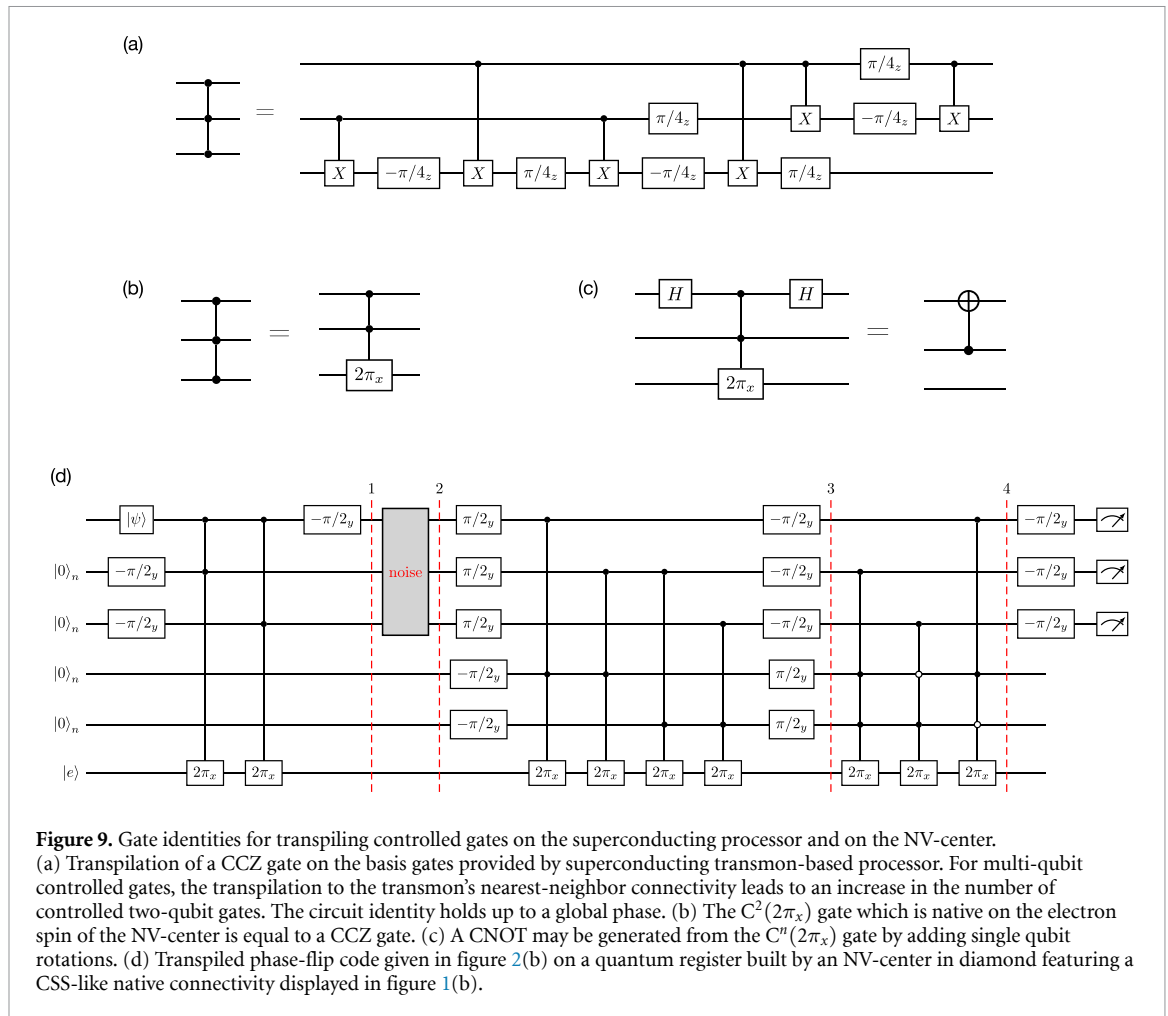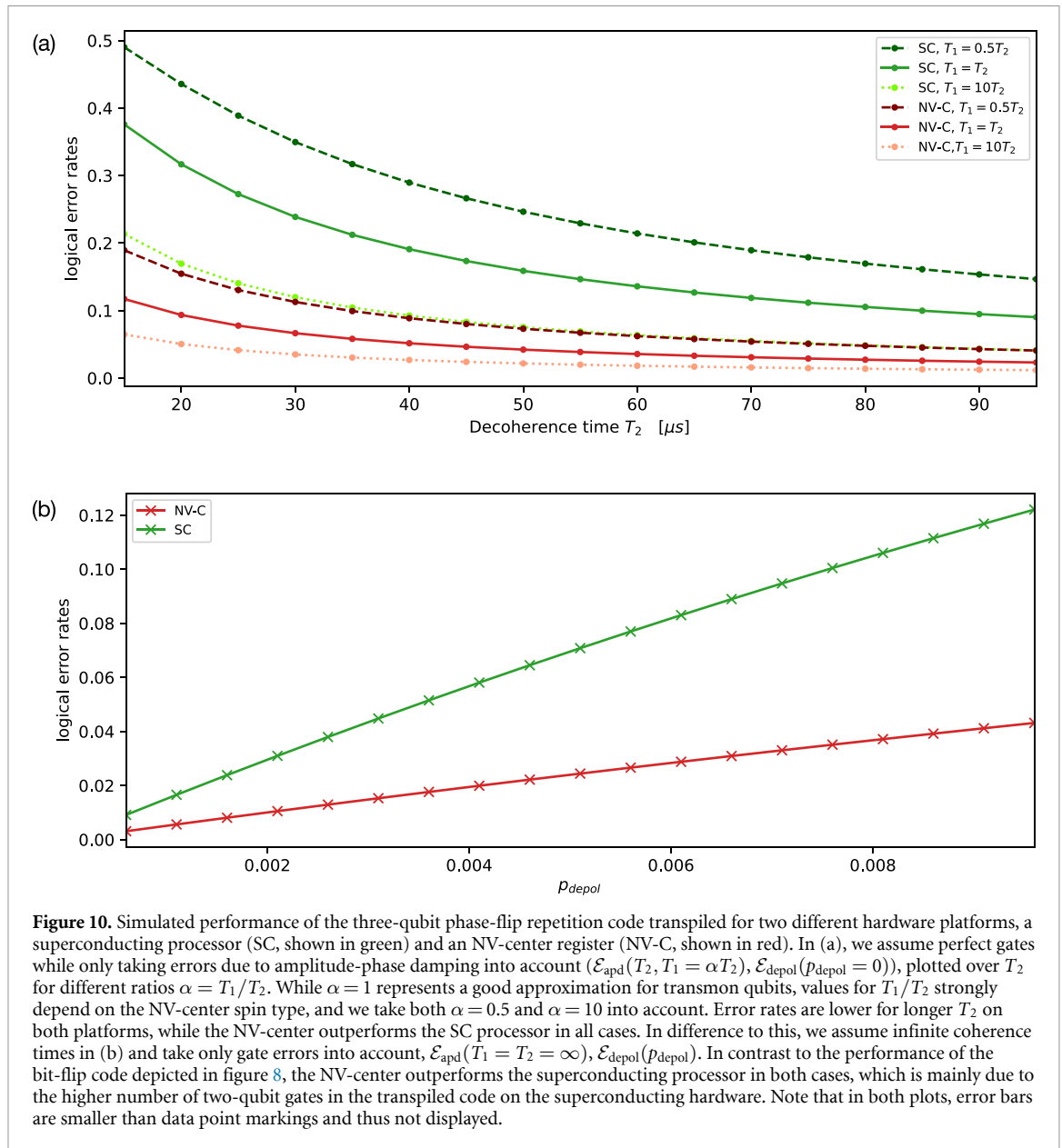
Figure 9. Gate identities for transpiling controlled gates on the superconducting processor and on the NV-center.
(a) Transpilation of a CCZ gate on the basis gates provided by superconducting transmon-based processor. For multi-qubit controlled gates, the transpilation to the transmon's nearest-neighbor connectivity leads to an increase in the number of controlled two-qubit gates. The circuit identity holds up to a global phase. (b) The $C^2(2\pi_x)$ gate which is native on the electron spin of the NV-center is equal to a CCZ gate. (c) A CNOT may be generated from the $C^n(2\pi_x)$ gate by adding single qubit rotations. (d) Transpiled phase-flip code given in figure 2(b) on a quantum register built by an NV-center in diamond featuring a CSS-like native connectivity displayed in figure 1(b).

transpile the circuit onto both platforms. As $C^{(2)}$-gates are not native on the superconducting platforms with nearest-neighbor coupling, they have to be translated into $C^{(1)}$-gates. With the set of basis gates provided by the transmon qubits, a CCZ-gate transpiles at the cost of 6 $C^{(1)}$ gates, see figure 9(a) [120–122]. This shows that for multi-qubit controlled gates, the transpilation to the transmon's nearest-neighbor connectivity leads to an increase in the number of controlled two-qubit gates. Also, additional swapping operations are needed due to the limited connectivity of the hexagonal layout, adding up to the number of CNOT gates in the circuit. In contrast to this, a CCZ-gate on the electron spin controlled by nuclear spins is native in the case of the NV-center. This gate may be used to create arbitrary controlled rotations between the nuclear spins using the gate identities depicted in figures 9(b) and (c).

As described in section 3.1, we compare the performance of the two circuits by taking gate errors as well as damping errors into account. Again, we first assume perfect gates and errors due to amplitude-phase damping ($\mathcal{E}_{\mathrm{apd}}(T_2, T_1 = \alpha T_2)$, $\mathcal{E}_{\mathrm{depol}}(p_{\mathrm{depol}} = 0)$), see figure 10(a), plotted over T_2 for different ratios $\alpha = T_1/T_2$. While $\alpha = 1$ represents a good approximation for transmon qubits, values for T_1/T_2 strongly depend on the NV-center spin type, and we take both $\alpha = 0.5$ and $\alpha = 10$ into account. In figure 10(b), we plot the case of infinite coherence times and imperfect gates. In contrast to the performance of the bit-flip code depicted in figure 8, the NV-center outperforms the superconducting processor in all cases. A predominant reason for this difference in performance are the different numbers of multi-qubit gates in the transpiled circuits, which are one of the main bottlenecks for the code performance on both platforms. The transpiled code for the NV-center is depicted in figure 9(d). The number of controlled gates is much smaller compared to the transpiled bit-flip code on the transmon processor which transpiles with 35 CNOTs (see figure B1 in appendix B).

Figure 10. Simulated performance of the three-qubit phase-flip repetition code transpiled for two different hardware platforms, a superconducting processor (SC, shown in green) and an NV-center register (NV-C, shown in red). In (a), we assume perfect gates while only taking errors due to amplitude-phase damping into account ($\mathcal{E}_{\mathrm{apd}}(T_2, T_1 = \alpha T_2)$, $\mathcal{E}_{\mathrm{depol}}(p_{\mathrm{depol}} = 0)$), plotted over T_2 for different ratios $\alpha = T_1/T_2$. While $\alpha = 1$ represents a good approximation for transmon qubits, values for T_1/T_2 strongly depend on the NV-center spin type, and we take both $\alpha = 0.5$ and $\alpha = 10$ into account. Error rates are lower for longer T_2 on both platforms, while the NV-center outperforms the SC processor in all cases. In difference to this, we assume infinite coherence times in (b) and take only gate errors into account, $\mathcal{E}_{\mathrm{apd}}(T_1 = T_2 = \infty)$, $\mathcal{E}_{\mathrm{depol}}(p_{\mathrm{depol}})$. In contrast to the performance of the bit-flip code depicted in figure 8, the NV-center outperforms the superconducting processor in both cases, which is mainly due to the higher number of two-qubit gates in the transpiled code on the superconducting hardware. Note that in both plots, error bars are smaller than data point markings and thus not displayed.

4. Discussion

Our findings also provide insights for the implementation of larger codes which fully correct one logical qubit, as for instance the 5-qubit code, the surface code, or the Steane color code, and for fault-tolerant QEC schemes.

First, the CSS-like connectivity is potentially advantageous for fault-tolerant stabilizer codes including flag qubits, as CNOT^n-gates (multi-qubit gates acting on n qubits controlled by the same qubit) play a significant role during encoding and parity check measurements—this connectivity is provided by the CSS. The high-fidelity execution of electron-controlled rotations of several nuclear spins simultaneously has recently been predicted [123]. Thus, even codes relying on high-weight parity-checks could provide promising (pseudo)-thresholds. Fault-tolerant operations for the $[5, 1, 3]$ code have been demonstrated on an NV-center already recently [33], while another promising candidate is the $[7, 1, 3]$ Steane code. These QEC schemes are best implemented on small systems with a few qubits, while for scalable architectures, they might prove advantageous in concatenated schemes relying on several NV-centers coupled via the electron spins. Secondly, the NV-center native CCPhase-gate—which is, up to single qubit rotations, equivalent to a Toffoli gate—offers two fundamentally important possibilities: Its application results in an all-to-all connectivity, as the 2π-rotation on the electron spin can be conditioned on the state of any two nuclear

qubits [69]. Using it to implement a unitary correction may prove advantageous compared to a measurement-based correction, depending on readout times and errors. Further, its transversal implementation in fault-tolerant schemes has been shown [55]. Given that the Toffoli gate together with the single-qubit Hadamard gate forms a universal set of quantum gates [124], it being a native gate on the NV-center also promises a favorable transpilation of many quantum algorithms onto NV-center based registers. Thirdly, we find that the heavy hexagonal layout of the superconducting processor proves advantageous in case the code is relying on a two-dimensional lattice connectivity such as the surface code. Also, in case of small codes relying on multi-qubit gates with multiple control as well as multiple target qubits, the codes potentially may be mapped to a linear or nearly-linear connectivity.

With respect to the influence of the connectivity maps, we summarize our findings as follows. The CSS connectivity is advantageous in the case of codes relying on parity checks on one ancilla qubit, as it is the case for stabilizer codes relying on flag qubits for fault-tolerance. More generally, whenever multi-qubit controlled gates are involved, the CSS topology allows for an advantageous transpilation. This is also relevant in an algorithms context where the CSS connectivity allows for efficient swapping routines [84, 125]. If, however, the two-qubit gates require connections involving many different control and target qubits, the quasi-linear, hexagonal layout is advantageous.

5. Conclusions

We compared the performance of quantum error-correcting codes on hardware platforms with different coherence times, connectivity, and native gates: a transmon qubit-based processor and an NV-center quantum register. For this, we used the repetition code correcting either a single bit-flip or a single phase-flip and transpiled them onto both hardware platforms. Additionally, we investigated different methods for replacing the feed-forward operation. Running the code on a superconducting processor, we benchmarked an error model which captures calibrated hardware properties and is thus adaptable to specific quantum processors. We used this model to simulate the impact of amplitude-phase damping and gate errors on the logical error rate for both hardware platforms. While the bit-flip code with post-processing leads to better logical error rates on the superconducting hardware, the phase-flip code with unitary correction shows much better performance on the NV-center register. A predominant reason for this difference in performance lies in the different numbers of multi-qubit gates in the transpiled circuits, which are one of the main bottlenecks for the code performance on both platforms. This strongly indicates that for smaller codes, the quasi-linear layout is advantageous, while for codes involving multi-qubit controlled operations, for instance high-weight parity checks, the native gate set and connectivity of the NV-center allow for a better correction. As multi-qubit controlled operations play an important role in many codes and algorithms, future directions of research could exploit the potential of this property for error correction of CSS-like systems or for designing efficient algorithms tailored to them.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

Acknowledgments

Appendix A. Kraus operators for amplitude-phase damping

In this section, we derive a set of Kraus operators for the combined process of amplitude and phase damping $\mathcal{E}_{\mathrm{apd}}(\rho)$.

Amplitude damping $\mathcal{E}_{\mathrm{ap}}(\rho)$ describes the effect of energy dissipation into the environment of a qubit [57, 103]. Its operators couple to the x–y plane of the Bloch sphere and cause a longitudinal relaxation to a certain steady state with

$$E_{\mathrm{ad},0} = \begin{pmatrix} 1 & 0 \\ 0 & \sqrt{1-p_{\mathrm{ad}}} \end{pmatrix}, \quad E_{\mathrm{ad},1} = \begin{pmatrix} 0 & \sqrt{p_{\mathrm{ad}}} \\ 0 & 0 \end{pmatrix}, \tag{A.1}$$

where p_{ad} represents the probability for the qubit to loose an excitation into the environment.

Phase damping $\mathcal{E}_{\mathrm{pd}}(\rho)$ describes the loss of information about the relative phases between the energy eigenstates into an environment, but does not affect the eigenstates themselves. In a simple model, it may be described by random phase kicks with a Gaussian-distributed variable. One possible set of its Kraus operators is given by

$$E_{\mathrm{pd},0} = \begin{pmatrix} 1 & 0 \\ 0 & \sqrt{1-p_{\mathrm{pd}}} \end{pmatrix}, \quad E_{\mathrm{pd},1} = \begin{pmatrix} 0 & 0 \\ 0 & \sqrt{p_{\mathrm{pd}}} \end{pmatrix}. \tag{A.2}$$

The set of Kraus operators for two combined quantum operations $\mathcal{E}_A$ and $\mathcal{E}_B(\rho)$ described by a set of Kraus operators $\{E_{A,j}\}$, $\{E_{B,i}\}$ and acting non-trivially on the same Hilbert space $\mathcal{H}_{AB}$ may be obtained according to

$$\mathcal{E}_A \circ \mathcal{E}_B(\rho) = \sum_j E_{A,j} \left(\sum_i E_{B,i} \rho E_{B,i}^\dagger \right) E_{A,j}^\dagger. \tag{A.3}$$

Calculating $\mathcal{E}_{\mathrm{apd}}(\rho) = \mathcal{E}_{\mathrm{pd}} \circ \mathcal{E}_{\mathrm{ad}}(\rho)$ leads to the set of Kraus operators [104]

$$E_{\mathrm{apd},0} = \begin{pmatrix} 1 & 0 \\ 0 & \sqrt{1-p_{\mathrm{ad}}}\sqrt{1-p_{\mathrm{pd}}} \end{pmatrix}, E_{\mathrm{apd},1} = \begin{pmatrix} 0 & \sqrt{p_{\mathrm{ad}}} \\ 0 & 0 \end{pmatrix}, \tag{A.4}$$

$$E_{\mathrm{apd},2} = \begin{pmatrix} 0 & 0 \\ 0 & \sqrt{1-p_{\mathrm{ad}}}\sqrt{p_{\mathrm{pd}}} \end{pmatrix} \tag{A.5}$$

where we may relate $p_{\mathrm{ad}}, p_{\mathrm{pd}}$ to the relaxation time T_1, the dephasing time T_2 and the gate time Δt with

$$1-p_{\mathrm{ad}} = e^{-\Delta t/T_1}, \sqrt{1-p_{\mathrm{ad}}}\sqrt{1-p_{\mathrm{pd}}} = e^{-\Delta t/T_2}. \tag{A.6}$$

While the reverse order $\mathcal{E}'_{\mathrm{apd}}(\rho) = \mathcal{E}_{\mathrm{ad}} \circ \mathcal{E}_{\mathrm{pd}}(\rho)$ leads to a different set of Kraus operators, their effect on the quantum state is identical, thus $\mathcal{E}_{\mathrm{apd}}(\rho) = \mathcal{E}'_{\mathrm{apd}}(\rho)$. This can be seen by calculating their unique Choi representation $J(\rho)$, which is related to the Kraus representation with
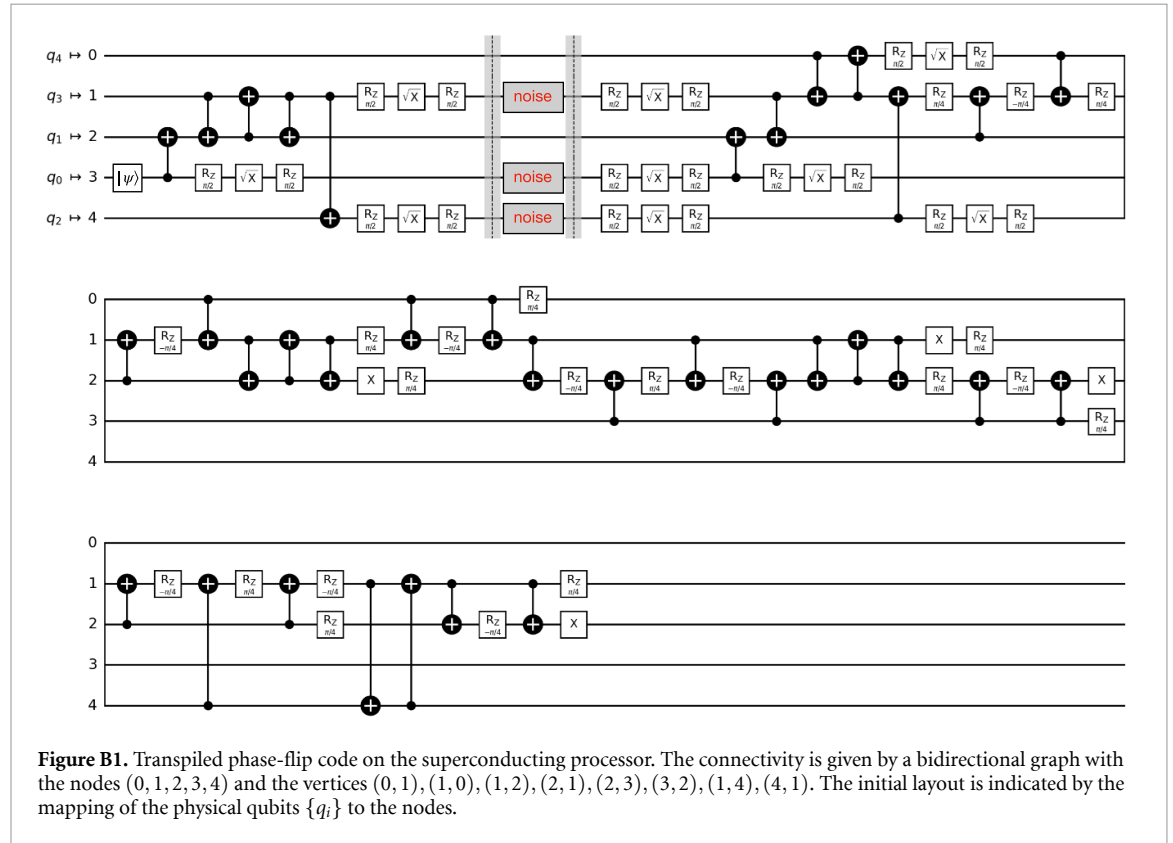
$$J(\rho) = \sum_k \mathrm{vec}(E_k)\mathrm{vec}(E_k^\dagger) \tag{A.7}$$

where $\mathrm{vec}(\cdot)$ represents the vectorization operation [107]. With this, we calculate

$$J(\mathcal{E}_{\mathrm{apd}}(\rho)) = J(\mathcal{E}'_{\mathrm{apd}}(\rho)) \tag{A.8}$$

$$= \begin{pmatrix} 1 & 0 & 0 & \sqrt{1-p_{\mathrm{ad}}}\sqrt{p_{\mathrm{pd}}} \\ 0 & p_{\mathrm{ad}} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \sqrt{1-p_{\mathrm{ad}}}\sqrt{p_{\mathrm{pd}}} & 0 & 0 & 1-p_{\mathrm{ad}} \end{pmatrix}. \tag{A.9}$$

Appendix B. Transpiled phase-flip code on the superconducting hardware

Figure B1. Transpiled phase-flip code on the superconducting processor. The connectivity is given by a bidirectional graph with the nodes $(0, 1, 2, 3, 4)$ and the vertices $(0, 1), (1, 0), (1, 2), (2, 1), (2, 3), (3, 2), (1, 4), (4, 1)$. The initial layout is indicated by the mapping of the physical qubits $\{q_i\}$ to the nodes.

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